

## OPERATING A MEMORY DEVICE

### Abstract of the Disclosure

A floating gate transistor has a reduced barrier energy at an interface with an  
5 adjacent gate insulator, allowing faster charge transfer across the gate insulator at lower  
voltages. Data is stored as charge on the floating gate. The data charge retention time  
on the floating gate is reduced. The data stored on the floating gate is dynamically  
refreshed. The floating gate transistor provides a dense and planar dynamic electrically  
alterable and programmable read only memory (DEAPROM) cell adapted for uses such  
10 as for a dynamic random access memory (DRAM) or a dynamically refreshed flash  
EEPROM memory. The floating gate transistor provides a high gain memory cell and  
low voltage operation.